

**In the Claims:**

1-40. (cancelled)

41. (previously presented) A system comprising:

A. a microphone having output leads;

B. a speaker having input leads: and

C. a processor including:

i. a semiconductor chip having microphone input leads connected to the microphone output leads and having speaker output leads connected to the speaker input leads;

ii. a processor formed on the chip and coupled to the microphone input leads and the speaker output leads, the processor including an ALU and selected registers that are associated with the ALU, each selected register being formed of a pair of first and second registers, the ALU storing program data in one of the first and second registers for each selected register;

iii. a context change signal lead formed on the semiconductor chip, the context change signal lead carrying a signal having a first state indicating a context of a first set of program instructions operating on first data stored in the selected registers and a second state indicating a context of a second set of program instructions operating on second data stored in the selected registers; and

iv. context switching circuitry formed on the semiconductor chip, the context switching circuitry being connected to the selected registers and the context change signal lead, the context change switching circuitry connecting one of the pair of first and second registers, for each selected register, to hold the first data in response to the first state of the context change signal and connecting the other of the pair of first and second

registers, for each selected register, to hold the second data in response to the second state of the context change signal.

42. (previously presented) The system of claim 41 in which the selected registers include an accumulator, an accumulator buffer, an auxiliary register, a compare register, an index register, a processor mode status register, a product register, a status register 0, a status register 1, a temporary register for multiplier, a temporary register for shift count and a temporary register for bit test.

43. (previously presented) The system of claim 41 in which the context change signal lead receives a hardware interrupt signal forming the context change signal.

44. (previously presented) The system of claim 41 in which the context change signal lead receives a signal indicating one of an interrupt, a software trap, and a subroutine.

45. (previously presented) The system of claim 41 in which the processor includes a hardwired multiplier coupled to the ALU.

46. (previously presented) The system of claim 41 in which each selected register includes the first register having an output connected to the input of the second register and the second register having an output connected to the input of the first register and the context switching circuitry moving the first data from the first register to the second register for each selected register.

47. (previously presented) The system of claim 41 in which each selected register includes the first and second register both having an input coupled to receive data from

the ALU and the context switching circuitry changes the flow of data being received by a selected register from the first register to the second register.

48. (previously presented) The system of claim 41 in which the context switching circuitry includes a multiplexer selectively switching data from the ALU to the first and second registers of each selected register.

49. (previously presented) The system of claim 41 in which the context switching circuitry includes a clock signal connected to each first and second register of each selected register selectively to clock data from the ALU into one and the other of the first and second registers.

50. (previously presented) The system of claim 41 in which the selected registers include an accumulator and a product register.

51. (previously presented) The system of claim 41 including an analog to digital converter connected between the microphone and the processor and a digital to analog converter connected between the processor and the speaker.